University of Wisconsin - Madison  
College of Engineering [EGR]  
Last Offered: 2015-2016 Spring [1164]  
Direct Link to this Syllabus :  
http://aefis.wisc.edu/index.cfm/page/CourseAdmin.ViewABET?coursecatalogid=64&pdf=True  

1. E C E 551, Digital System Design and Synthesis  
2. Credits : 3  
   Contact Hours : 3.5  
3. Textbook and Materials: Verilog HDL: a guide to digital design synthesis; Palnitkar; 2nd; 2003  
   a. Other Supplemental Materials: None  

   • Specific Course Information:  
      a. Brief description of the content of the course (Course Catalog Description):  
      b. Pre-requisites or Co-requisites: ECE/Comp Sci 352 & Jr st  
      c. This is a Selected Elective course.  

   • Specific Goals for the Course:  
      a. Course Outcomes:  
         1. Develop ability to use a hardware description language, simulation, and a logic synthesis tool in the design and verification of digital circuits  
         2. Understand design in a contemporary environment resulting from the use of deep-submicrometer implementation technologies and design reuse.  

   • ABET Student Learning Outcomes:
(a) Ability to apply mathematics, science and engineering principles.
(b) Ability to design and conduct experiments, analyze and interpret data.
(c) Ability to design a system, component, or process to meet desired needs.
(e) Ability to identify, formulate and solve engineering problems.
(g) Ability to communicate effectively.
(j) Knowledge of contemporary issues.
(k) Ability to use the techniques, skills and modern engineering tools necessary for engineering practice.

- Brief List of Topics to be Covered:

  REVIEW OF COMBINATIONAL AND SEQUENTIAL LOGIC DESIGN

  STRUCTURAL MODELS OF COMBINATIONAL LOGIC

  LOGIC SIMULATION

  PROPAGATION DELAY

  USER DEFINED PRIMITIVES

  BEHAVIORAL MODELS OF COMBINATIONAL AND SEQUENTIAL LOGIC

  SYNTHESIS OF COMBINATIONAL AND SEQUENTIAL LOGIC

  DESIGN AND SYNTHESIS OF DATAPATH CONTROLLERS

  ARITHMETIC PROCESSORS

  POSTSYNTHESIS DESIGN TASKS